UNIVERSITÀ DI PISA

**DIPARTIMENTO DI INGEGNERIA DELL'INFORMAZIONE**

**Dottorato di Ricerca in Ingegneria dell'Informazione**

Doctoral Course

# "Design Technologies for Embedded Multiprocessor Systems-on-Chip"

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**Short Abstract:** Virtually all digital IC platforms today are based on flexible programmable processor cores, with a trend towards Multi/Manycore architectures comprising 10-100 cores. This trend is imposed by high performance and power/energy efficiency demands. Specifically in competitive embedded application domains like smartphones, wireless infrastructure, and automotive, there are tight efficiency constraints on power, energy, timing, design cost, and production cost of the underlying HW platforms. The need for flexibility and efficiency leads to heterogeneous platform architectures, composed of off-the-shelf (yet partially customizable) IP cores, like RISCs, and custom application-specific processors, such as DSP or security accelerators. Moreover, these cores communicate over complex on-chip interconnect and memory subsystem architectures. These trends impose huge challenges for ICT system and semiconductor industry. Novel design methodologies and tools are required for managing the skyrocketing HW platform design complexity, while simultaneously optimizing systems and components for performance, power, and costs. Furthermore, migrating legacy application software code or firmware as well as developing and debugging new software for highly parallel HW platforms causes a significant design productivity gap. This course presents various advanced system-level design methodologies in a practice-oriented way, intended to enable industrial embedded systems engineers to manage the complexity of current and future HW/SW multicore devices and to achieve predictable and competitive results in shorter time. Topics include: Software compilation techniques, System-on-Chip design methodology, power optimization, Virtual Prototyping and simulation, and Application Specific Processor Design. Furthermore, a brief outlook on hardware security issues will be provided.

**Course Contents in brief:**

- Multiprocessor Systems-on-Chip
- Electronic System Level Design
- SoC architecture exploration and power estimation
- Virtual Prototyping
- Multicore programming tools
- Application-specific processing elements (ASIPs)

**Total # of hours of lecture**: 20

**References:**

R. Leupers: Code Optimization Techniques for Embedded Processors – Methods, Algorithms, and Tools, Kluwer Academic Publishers, ISBN 0-7923-7989-6, Nov 2000

A. Hoffmann, H. Meyr, R. Leupers: Architecture Exploration for Embedded Processors with LISA, Kluwer Academic Publishers, ISBN 1-4020-7338-0, Dec 2002

P. Ienne, R. Leupers (eds.): Customizable Embedded Processors: Design Technologies and Applications, Morgan Kaufmann, Series in Systems on Silicon, ISBN 0-1236-9526-0, Jul 2006

J. Castrillon, R. Leupers: Programming Heterogeneous MPSoCs: Tool Flows to Close the Software Productivity Gap, Springer, ISBN 978-3319006741, July 2013

S. Bhattacharyya, E. Deprettere, R. Leupers, J. Takala (eds.): Handbook of Signal Processing Systems, 3rd Edition, Springer, ISBN 978-3-319-91733-7, Oct 2018

S. Schuermans, R. Leupers: Power Estimation on Electronic System Level using Linear Power Models, Springer, ISBN 978-3-030-01875-7, Jan 2019

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**CV of the Teacher**

Rainer Leupers received the M.Sc. (Dipl.-Inform.) and Ph.D. (Dr. rer. nat.) degrees in Computer Science with honors from TU Dortmund in 1992 and 1997. From 1997-2001 he was the Chief Engineer at the Embedded Systems Chair at TU Dortmund. In 2002, he joined RWTH Aachen University as a professor for Software for Systems on Silicon. His research comprises embedded software development tools, multicore processor architectures, hardware security, and system-level electronic design automation. He served in committees of the leading international EDA conferences and received various scientific awards, including Best Paper Awards at DAC and twice at DATE, as well as several industrial awards. Dr. Leupers is also engaged as an entrepreneur and in turning research results into innovations. He holds several patents and has been a co-founder of LISATek (now with Synopsys), Silexica, and Secure Elements. As the coordinator of the TETRACOM and TETRAMAX projects, he contributes to EU-wide academia-to-industry technology transfer.

**Room and Schedule**

Room: *Aula Riunioni del Dipartimento di Ingegneria dell'Informazione, Via G. Caruso 16, Pisa – Ground Floor*

Schedule:

July 14-17, 2020

| | Tue 14 | Wed 15 | Thu 16 | Fri 17 |
|---|---|---|---|---|
| **09:30-11:00** | | Lecture 3 | | final test |
| **11:00-11:30** | | break | Lab 3 | |
| **11:30-13:00** | | Lecture 4 | Lecture 5 | |
| **13:00-14:00** | | lunch break | lunch break | |
| **14:00-15:30** | Lecture 1 | Lab 1 | Lecture 6 | |
| **15:30-16:00** | break | break | break | |
| **16:00-17:30** | Lecture 2 | Lab 2 | Lab 4 | |